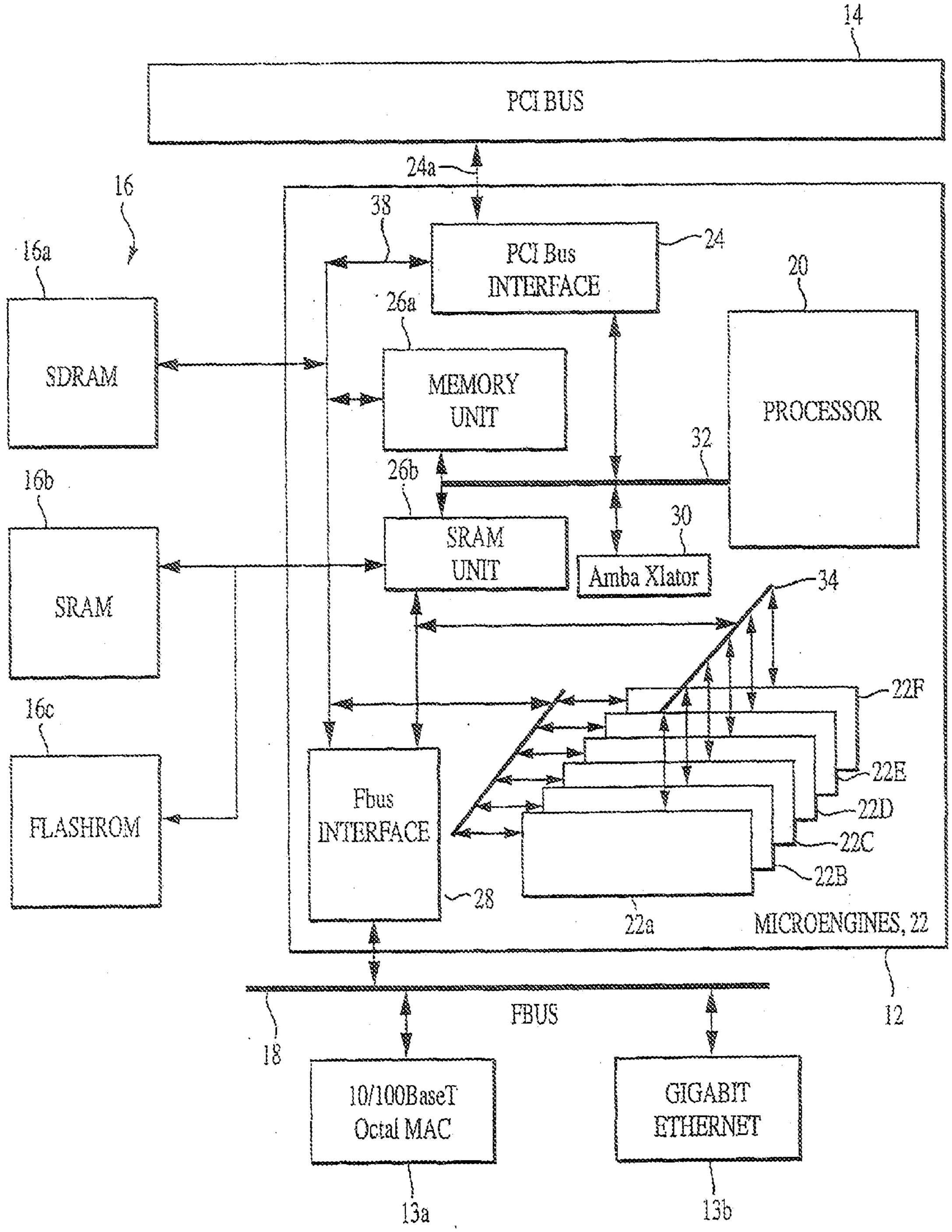
14
PCI BUS
24a
16
38
24
PCI Bus INTERFACE
20
16a
26a
SDRAM
MEMORY UNIT
PROCESSOR
32
26b
16b
30
SRAM UNIT
SRAM
Amba Xlator
34
22F
16c
22E
Fbus INTERFACE
22D
FLASHROM
22C
22B
28
22a
MICROENGINES, 22
FBUS
12
18
10/100BaseT Octal MAC
GIGABIT ETHERNET
13a
13b

FIG. 1

REPLACEMENT SHEET

Appln No.: 10/070,006

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Applicant(s): Gilbert Wolrich et al.

DOUBLE SHIFT INSTRUCTION FOR MICRO ENGINE USED IN MULTITHREADED PARALLEL PROCESSOR ARCHITECTURE

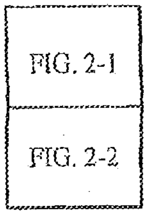


FIG. 2

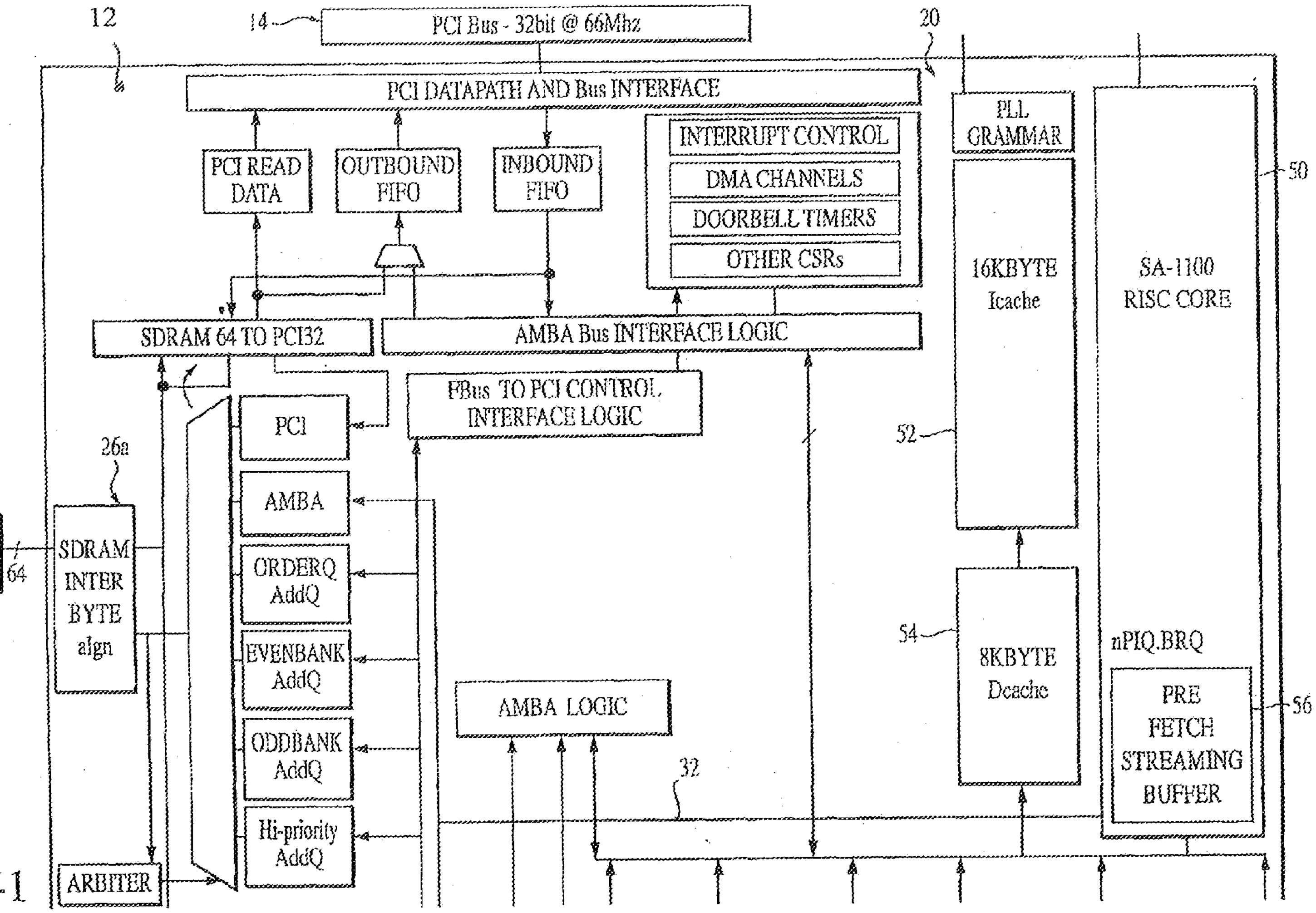


FIG. 2-1

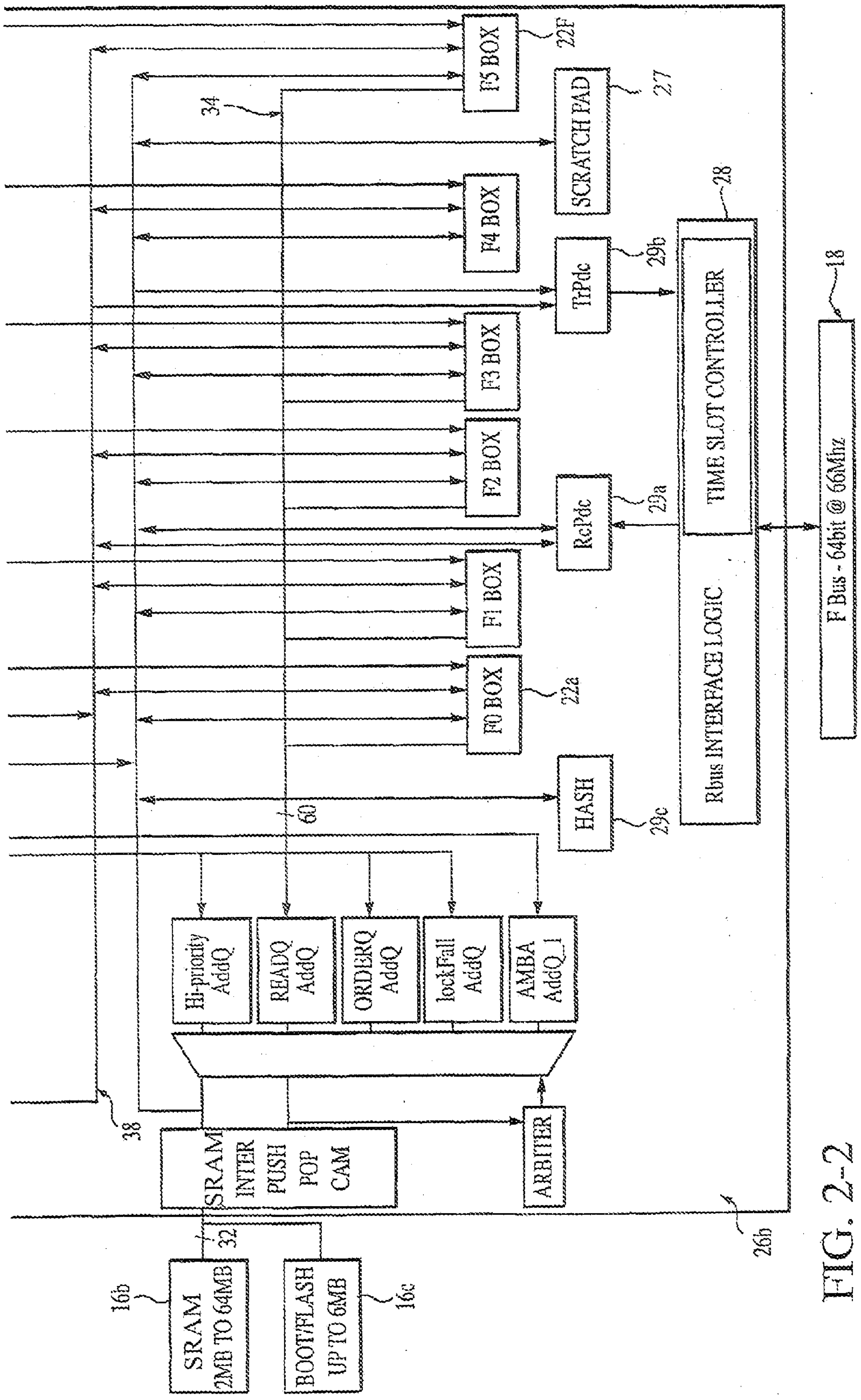

F5 BOX
22F
SCRATCH PAD
27
34
F4 BOX
28
TrPdc
29b
TIME SLOT CONTROLLER
18
F3 BOX
F2 BOX
RcPdc
29a
F1 BOX
F0 BOX
22a
Rbus INTERFACE LOGIC
F Bus - 64bit @ 66Mhz
HASH
29c
60
Hi-priority AddQ
READQ AddQ
ORDERQ AddQ
lockFail AddQ
AMBA AddQ_1
38
SRAM INTER PUSH POP CAM
ARBITER
26b
32
SRAM 2MB TO 64MB
16b
BOOT/FLASH UP TO 6MB
16c

FIG. 2-2

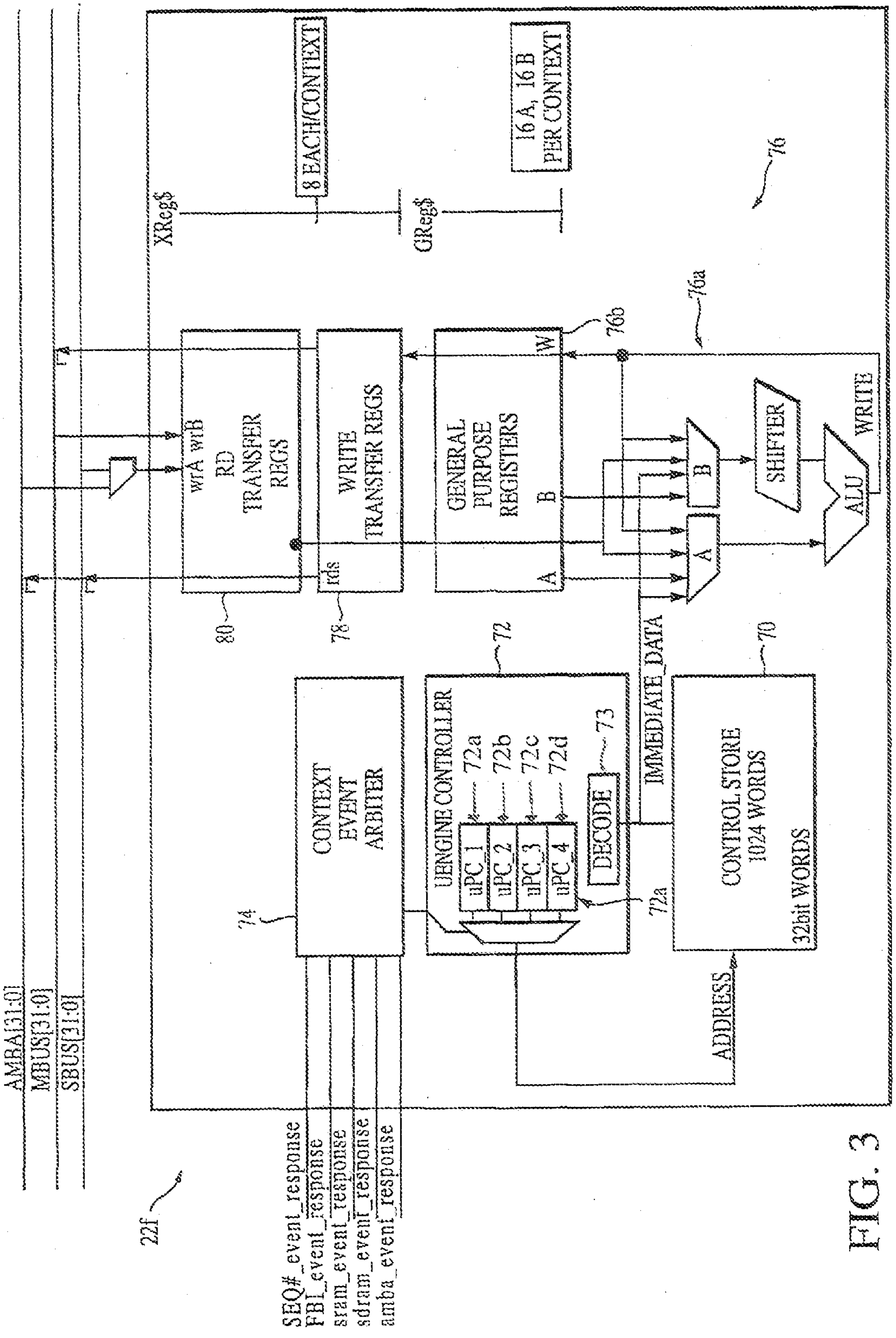

AMBA[31:0]
MBUS[31:0]
SBUS[31:0]
22f
XReg$
8 EACH/CONTEXT
GReg$
16 A, 16 B
PER CONTEXT
76
76a
76b
wrA wrB
RD
TRANSFER
REGS
80
WRITE
TRANSFER REGS
rds
78
GENERAL
PURPOSE
REGISTERS
B
A
W
A
B
SHIFTER
ALU
WRITE
IMMEDIATE_DATA
CONTEXT
EVENT
ARBITER
74
UENGINE CONTROLLER
72
uPC_1
uPC_2
uPC_3
uPC_4
72a
72b
72c
72d
DECODE
73
72a
CONTROL STORE
1024 WORDS
32bit WORDS
70
ADDRESS
SEQ#_event_response
FBI_event_response
sram_event_response
sdram_event_response
amba_event_response

FIG. 3

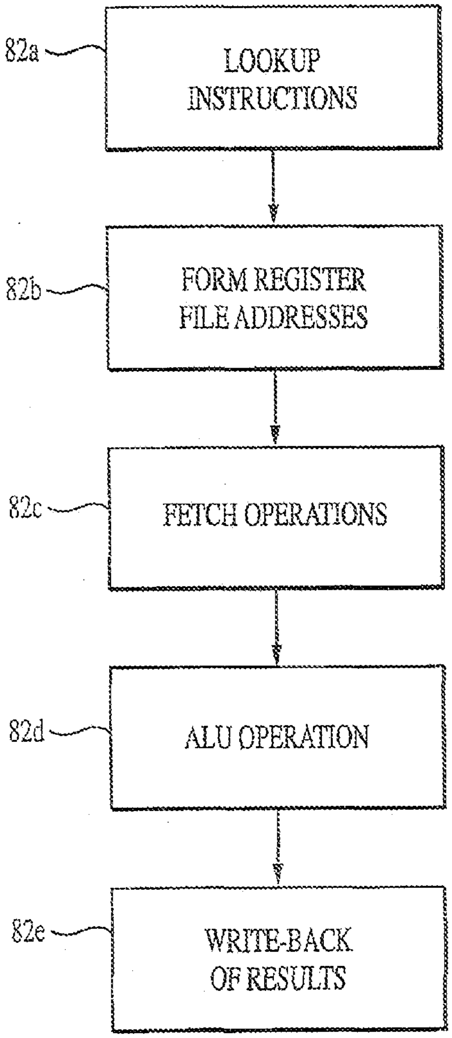
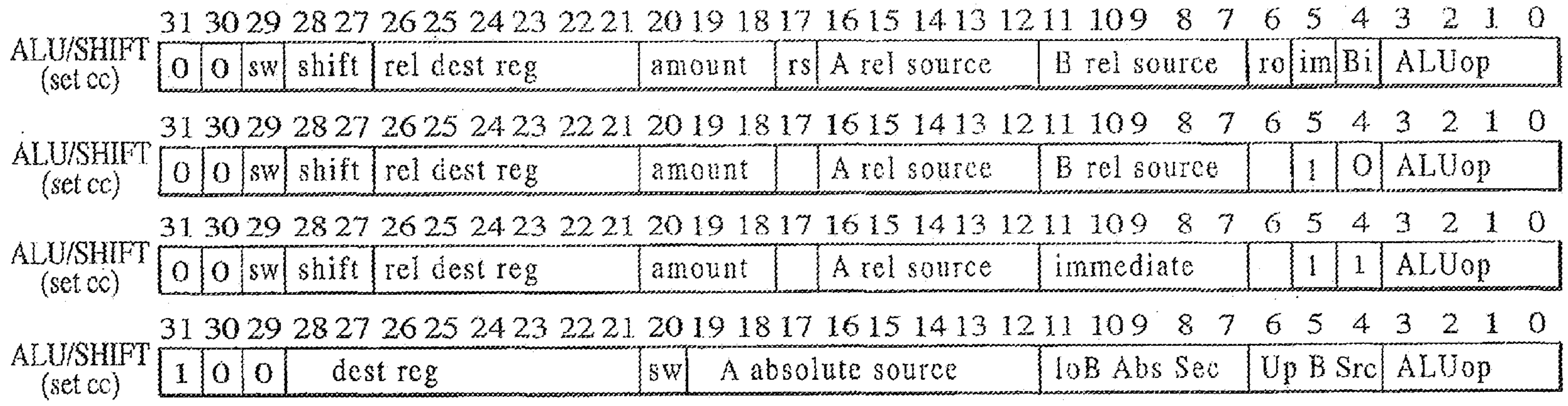

82a
LOOKUP INSTRUCTIONS
82b
FORM REGISTER FILE ADDRESSES
82c
FETCH OPERATIONS
82d
ALU OPERATION
82e
WRITE-BACK OF RESULTS

FIG. 4



Shift Decode:

(rs,r0) decode ([31:0] shifts into [63:32] and take [63;32]):

00 = left rotate
01 = right shift (32-ShfAmt = Right Shift Amt)
10 = left shift
11= double shift (upper A-op shifts into lower B-op)

===> "left rotate" of zero gives zero shift (therwise zero amount signifies indirect shift)

ALU-OP decode:

0000 = B	0100 = ~A&B (~and)	1000 = A-B	1100 = A+B(8)
0001 = ~B	0101 =XOR	1001 = B-A	1101 = A+B(16)
0010 = A&B (and)	0110 = OR	1010 =	1110 = A+B
0011= A&~B (and~)	0111= mul-stuff	1011=	0011= A+B+Cin

FIG. 5